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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/726,301	12/02/2003	Henry P. Moreton	NVDA P000572	3090

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EXAMINER	
SINGH, DALIP K	
ART UNIT	**PAPER NUMBER**
2676	

DATE MAILED: 02/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/726,301	MORETON ET AL.	
	Examiner	Art Unit	
	Dalip K Singh	2676	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 May 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5 and 7-21* is/are rejected.

7)☒ Claim(s) *6 and 22-25* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent Application Publication No. 2004/0143833 A1 to Heyrman et al. in view of U.S. Patent No. 6,058,460 to Nakhimovsky.

a. Regarding claim 1, Heyrman et al. **discloses** an apparatus, program product and method in which threads are dynamically assigned to computer resources based upon specific "types" associated with such threads (page 2, paragraph 0013, Summary of the Invention; page 2, paragraph 0025). However, Heyrman et al. **does not disclose** allocating memory spaces for data buffers accessible by the threads. Nakhimovsky **discloses** establishing memory pools in the system memory, mapping each thread to one of the memory pools (col. 1, lines 45-67). Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to modify the device as taught by Heyrman et al. with the feature "memory pools mapped to each thread" as taught by Nakhimovsky **because** it provides for threads executing with greater efficiency.

3. Claims 2-5 and 7-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent Application Publication No. 2004/0143833 A1 to Heyrman et al. in view of U.S. Patent No. 6,058,460 to Nakhimovsky as applied to claim 1 above, and further in view of U.S. Patent No. 6,631,462 B1 to Wolrich et al.

a. Regarding claim 2, Heyrman-Nakhimovsky **is silent about** one thread writing to a data buffer and that data buffer being read by another thread. Wolrich et al. **discloses** wherein microengine 22a sets aside a first active thread to process a second active thread and any microengine can assume the processing (col. 3, lines 10-18; col. 8, lines 5-18). Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to modify Heyrman-Nakhimovsky combination with the feature "different threads reading the same data buffer" as taught by Wolrich et al. **because** it provides for efficient management of active threads.

b. Regarding claim 3, Wolrich et al. **implicitly discloses** checking for a read-after-write hazard existence for a location in a memory space for a thread in that microengines 22 employ signaling states whereby an executing thread can broadcast a signal state (col. 4, lines 46-53). Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to modify Heyrman-Nakhimovsky combination with the feature "thread signaling state broadcast" as taught by Wolrich et al. **because** it results in efficient thread management.

c. Regarding claim 4, Wolrich et al. **discloses** wherein a position in a data buffer is determined by a thread (...an SRAM access requested by a Thread_0, from ...will cause...fetches the data from the SRAM 16b...col. 2, lines 49-67).

d. Regarding claim 5, Nakhimovsky **discloses** memory pools being identified by an index (col. 2, lines 39-50).

e. Regarding claim 7, Heyrman et al. **is silent about** data buffers and their different sizes. Nakhimovsky **discloses** establishing memory pools and the ability to manipulate its memory pool sizes. Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to modify Heyrman et al. with the feature "varying memory pool size" as taught by Nakhimovsky **because** it provides for greater efficiency.

f. Regarding claim 8, Heyrman-Nakhimovsky combination **is silent about** mutually exclusive workings of said first and second thread when accessing a first and second memory space, respectively and third memory space being accessed commonly by first and second threads. Wolrich et al. **discloses** multiple threads that are simultaneously active and independently work on a task, as well the concept of a two threads accessing the same shared resource (col. 1, lines 60-67; col. 3, lines 1-18). Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to modify Heyrman-Nakhimovsky combination with the feature "simultaneous active threads and working independently on a task in a mutually exclusive fashion" as taught by Wolrich et al. **because** it provides for better multithreading management.

g. Regarding claim 9, Nakhimovsky **discloses** establishing data buffers (memory pools) in the system memory, mapping each thread to one of the memory pools (col. 1, lines 45-67). Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to modify the device as taught by Heyrman et al. with the feature "memory pools mapped to each thread" as taught by Nakhimovsky **because** it provides for threads executing with greater efficiency.

h. Regarding claim 10, it is similar in scope to claim 4 above and is rejected under the same rationale.

i. Regarding claim 11, it is similar in scope to claim 3 above and is rejected under the same rationale.

j. Regarding claim 12, it is similar in scope to claim 2 above and is rejected under the same rationale.

k. Regarding claim 13, it is similar in scope to claim 5 above and is rejected under the same rationale.

l. Regarding claim 14, it is similar in scope to claim 8 above and is rejected under the same rationale.

m. Regarding claim 15, it is similar in scope to claim 12 above and is rejected under the same rationale.

n. Regarding claim 16, it is similar in scope to claim 3 above and is rejected under the same rationale.

o. Regarding claim 17, it is similar in scope to claim 14 above and is rejected under the same rationale.

p. Regarding claim 18, it is similar in scope to claim 13 above and is rejected under the same rationale.

4. Claims 19-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,630,935 B1 to Taylor et al. , in view of U.S. Patent No. 6,058,460 to Nakhimovsky.

a. Regarding claim 19, Taylor et al. **discloses** a memory resource (memory 16, Fig. 1), a graphics processor (computation engine 12) coupled to said memory resource, an address unit (arbitration module 14) (col. 4, lines 29-67; col. 5, lines 1-64). Taylor et al. **implicitly discloses** CPU in that a graphics processor in a video system has to interact with a CPU (...the input data 72 may correspond to the data generated by the central processing unit...col. 4,lines 65-67). Taylor et al. **is silent about** allocating a memory space to each thread as well an additional memory space accessible by each thread in a first set of threads. Nakhimovsky **discloses** allocating memory pools for each thread (col. 1, lines 45-67). Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to modify the device as taught by Heyrman et al. with the feature "memory pools mapped to each thread" as taught by Nakhimovsky **because** it provides for threads executing with greater efficiency.

b. Regarding claims 20 and 21, they are similar in scope to claim 11 above and is rejected under the same rationale.

Allowable Subject Matter

5. Claims 6 and 22-25 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Prior art while disclosing buffer identifier for a memory location determination fails to disclose position coordinates as a criteria associated with a sample for memory location address determination; prior art while disclosing data buffers with identifier fails to disclose each date buffer in the additional memory space being associated with a unique buffer identifier; address unit using the buffer identifier and sample position coordinates to determine if a read-after-write hazard exists.

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Dalip K. Singh** whose telephone number is **(703) 305-3895**. The examiner can normally be reached on Mon-Thu (8:00AM-6: 30PM) Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, **Matthew Bella**, can be reached at **(703) 308-6829**.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 872-9314 (for Technology Center 2600 only)

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

dks

February 7, 2005

MATTHEW C. BELLA
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600